



EK79632A EPD Driver

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S960/800/720/640*G640/600/540/480 EPD Driver

1. GENERAL DESCRIPTION

The EK79632A is an EPD IC max for 960*640 active matrix display, include Source driver and Gate driver. It also provides cascade function for dot expansion.

The Source driver is a selectable 960, 800, 720 or 640 bit long 2-bit wide serial-input parallel-output driver with level conversion on each parallel output which converts the 2 digital bits into positive, GND, or negative analog output voltages. An 8-bit input bus simultaneously inputs 4 groups of 2 bits each. It consists of a Bi-Directional Shift Data Inputs, Transfer Latch, and 960 bit Level Shifter/Output Driver. Each "S[1] .. S[960]" pin is switched to one of [VPOS, GND, VNEG], according to the D7...D0 logic levels clocked into the Source driver, modified by the OE pin.

After a start pulse of Gate driver is triggered, output pins will output high-driving voltage pulses sequentially for the gate signals of the display. It supports 640/600/540/480 channels, shift up/down selection.

2. FEATURES

Source

- CMOS Technology
- 960/800/720/640 Output Channels Selectable
- Drives Segment or Active Matrix Displays
- +/-15 Volt Source Output Driver Supply Voltage
- Logical Interface: 1.7V ~ 3.6V
- Maximum Operating Frequency: 60MHz / 45MHz (VCC = 2.5V ~ 3.6V / 1.7V ~ 2.5V)
- Bi-Directional Shift 8-bit Data Inputs

Gate

- 640/600/540/480 Output Channels Selectable
- Built-in Bi-direction Shift Register
- Logical Interface: 1.7V ~ 3.6V
- Output Supply Voltage : VGL + 45V
- Maximum Operation Frequency: 200KHZ
- CMOS Silicon Gate

Package

- COG type

3. BLOCK DIAGRAM

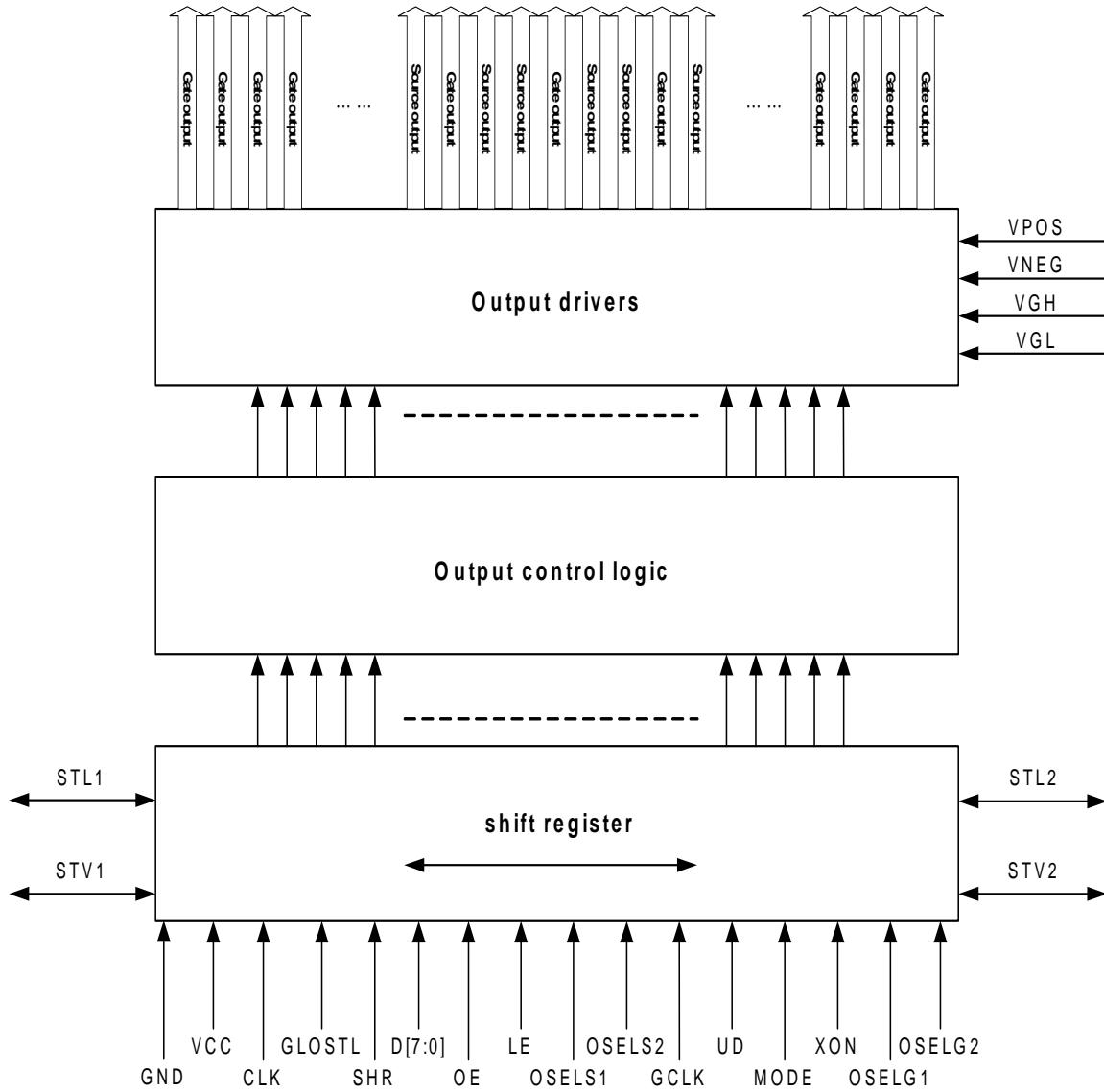


Figure 1. Block Diagram

4. PIN DESCRIPTION

Table 1. Pin Description

Pin Name	Pin Type	Description
Source Driver		
CLK	Input	Source driver clock input. Data inputs are captured on the rising edge of clock signal.
STL1	Bi-direction	SHR Start Pulse Input Start Pulse Output
STL2		H STL2 STL1
		L STL1 STL2
GLOSTL	Input with Pull High	Global start pulse input. SHR GLOSTL synchronous H First IC' STL2 L First IC' STL1 It is the same and synchronous with start pulse input in unity use. It is the same and synchronous with the first IC's start pulse input in cascade use.
SHR	Input	SHR= H: Data inputs read sequentially from S[960] to S[1]. SHR= L: Data inputs read sequentially from S[1] to S[960]. It is asynchronous to clock CLK.
D[7:0]	Input	Source driver data input pins. They are latched on the rising edge of CLK.
OE	Input with Pull Low	Source driver outputs enabled when OE is logic "H", Outputs forced to GND when OE is logic "L". It is asynchronous to clock CLK.
LE	Input	Source driver parallel latch enable, transparent when high. It is asynchronous to clock CLK.
S[1] ~ S[960]	Output	Source driver parallel outputs. Range is from VNEG to VPOS. Always drive to GND by setting OE to logic "L" prior to power switching on or off.
OSELS1 OSELS2	Input with Pull High	Source output channel select inputs. OSELS1 OSELS2 channels H H 960 H L 800 L H 720 L L 640
Gate Driver		
GCLK	Input	Gate driver shift clock pin. The shift register data is shifted synchronously with each rising edge of GCLK.
STV1	Bi-direction	UD Start Pulse Input Start Pulse Output
STV2		H STV1 STV2
		L STV2 STV1
UD	Input	Used as gate driver up/down pulse direction control and setting cascade sequence input pin. Display drive outputs shift from G[1] to G[640] when set to "H" Display drive outputs shift from G[640] to G[1] when set to "L".
MODE	Input with Pull Low	Used as gate driver output mode selection pins. MODE = H: Normal single pulse. MODE = L: Always keep VGL.

Pin Name	Pin Type	Description															
Gate Driver																	
XON	Input with Pull High	When XON input pin is 'L', all the output pins are forced to VGH level. Also it has an internal pull high resistor, keep it to VCC is preferred when unused. The chip internal shift register is not cleared when XON input is active.															
OSELG1 OSELG2	Input with Pull High	Gate output channel select inputs. <table border="1"> <thead> <tr> <th>OSELG1</th> <th>OSELG2</th> <th>channels</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>640</td> </tr> <tr> <td>H</td> <td>L</td> <td>600</td> </tr> <tr> <td>L</td> <td>H</td> <td>540</td> </tr> <tr> <td>L</td> <td>L</td> <td>480</td> </tr> </tbody> </table>	OSELG1	OSELG2	channels	H	H	640	H	L	600	L	H	540	L	L	480
OSELG1	OSELG2	channels															
H	H	640															
H	L	600															
L	H	540															
L	L	480															
G[1] ~ G[640]	Output	Gate driver output pins for driving the display's gate signals. The amplitude of these outputs is from VGH to VGL. The output timing of these signals is synchronous with the rising edge of the shift clock.															
Power Supply																	
VPOS	Power	Supply of positive power for source outputs															
VNEG	Power	Supply of negative power for source outputs															
VCC	Power	Power for digital circuit															
GND	Power	Ground pin															
VGH	Power	Supply of positive power for the gate outputs.															
VGL	Power	Supply of negative power for the gate outputs.															
Others																	
Others' pads which not be mentioned above	--	Please do not connect to any signal or power, just let them open.															

Note: SHR, UD and MODE can not be changed during frame.

5. FUNCTION DESCRIPTION

5.1. Description

The EK79632A is an EPD IC max for 960*640 active matrix display, include Source driver and Gate driver. It also provides cascade function for dot expansion.

The Source driver is a selectable 960, 800, 720 or 640 bit long 2-bit wide serial-input parallel-output driver with level conversion on each parallel output which converts the 2 digital bits into positive, GND, or negative analog output voltages. An 8-bit input bus simultaneously inputs 4 groups of 2 bits each.

Terminal SHR, when SHR = logic 1, the data inputs are read sequentially from S[960] to S[1] end of the device. The direction is reversed when SHR is logic 0. It is asynchronous to the clock CLK.

The two input terminals latch enable (LE) and output enable (OE) are asynchronous to the clock CLK. Terminal OE, when is logic 0, forces "S[1]...S[960]" outputs to GND. Terminal LE controls 960 latches that are transparent when LE is logic 1 and hold the data when LE is logic 0.

The EK79632A logic is static CMOS type. The current drain depends on the operating frequency.

Each "S[1]...S[960]" pin is switched to one of [VPOS, GND, VNEG] voltage levels according to the D[7:0] logic levels clocked into the EK79632A, modified by the OE pin. The truth tables are shown in the following tables.

Table 2. Data Input Truth Table (n = 0 to 3, k = 0 to 239)

OE	D [2n + 1]	D [2n]	SHR = H	SHR = L
			Output [n + 1 + 4k]	Output [4(k+1) - n]
1	0	0	GND	GND
1	0	1	VPOS	VPOS
1	1	0	VNEG	VNEG
1	1	1	GND	GND
0	X	X	GND	GND

Table 3. Source clock input Table

Output channels	Latch clocks	Dummy clocks	Total clocks
960	240	≥ 3	240 + Dummy clocks
800	200		200 + Dummy clocks
720	180		180 + Dummy clocks
640	160		160 + Dummy clocks

Note:

After the last data, it should append 3 dummy clocks at least.

Example1: If only 840 output channels in use, the total clocks should be 210+3 at least.

Example2: In cascade application, if output channels are 1920, the total clocks should be 480+3 at least.

5.2. Power On/Off Sequence

This IC is a high-voltage EPD driver, so it may be damaged by a large current flow if an incorrect power sequence is used. Connecting the drive powers, [VNEG, VGL] & [VPOS, VGH], after the logical power, VCC, is the recommended sequence. When shutting off the power, shut off the drive power and then the logic system or turn off all powers simultaneously.

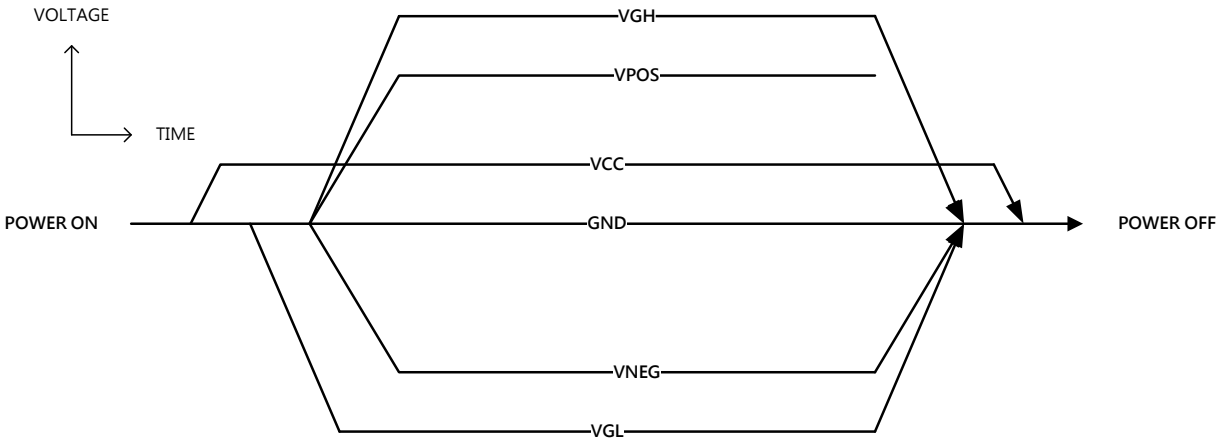


Figure 2. Power On/Off Sequence

5.3. Power Level

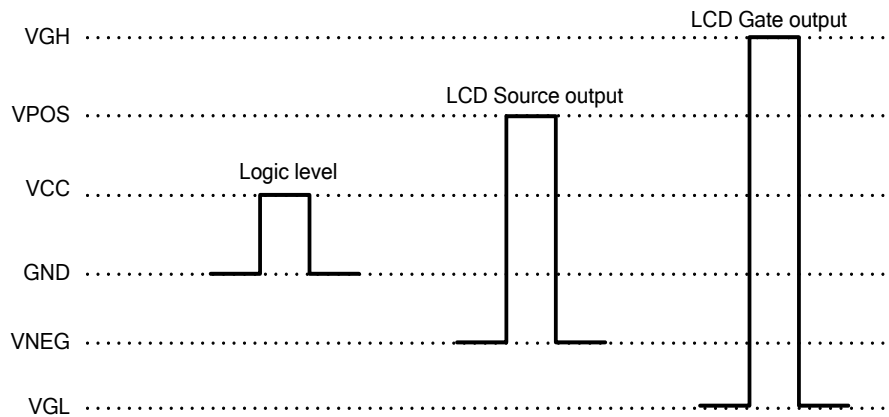


Figure 3. Signal voltage level

Note: For the input signals: CLK, STL1, STL2, GLOSTL, SHR, D[7:0], OE, LE, OSELS1, OSELS2, GCLK, STV1, STV2, UD, MODE, XON, OSELG1 and OSELG2 "High" level = VCC, "Low" level = GND.

5.4. Channel Selection Function

OSELS1	OSELS2	Source Output Channels	Valid Output Channels	Invalid Output Channels
H	H	960CH	S1 ~ S960	None
H	L	800CH	S1 ~ S400, S561 ~ S960	S401 ~ S560 Fix to GND
L	H	720CH	S1 ~ S360, S601 ~ S960	S361 ~ S600 Fix to GND
L	L	640CH	S1 ~ S320, S641 ~ S960	S321 ~ S640 Fix to GND
OSELG1	OSELG2	Gate Output Channels	Valid Output Channels	Invalid Output Channels
H	H	640CH	G1 ~ G640	None
H	L	600CH	G21 ~ G620	G1 ~ G20, G621 ~ G640 Fix to VGL
L	H	540CH	G51 ~ G590	G1 ~ G50, G591 ~ G640 Fix to VGL
L	L	480CH	G81 ~ G560	G1 ~ G80, G561 ~ G640 Fix to VGL

6. ELECTRICAL SPECIFICATION

6.1. Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings (GND = 0 V)

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	VCC	-0.3 to +5	V
Positive Supply Voltage	VPOS	-0.3 to +18	V
Negative Supply Voltage	VNEG	+0.3 to -18	V
Max. Drive Voltage Range	VPOS - VNEG	36	V
Supply voltage	VGH	-0.3 to + 46	V
Supply voltage	VGL	-25.0 to + 0.3	V
Supply range	VGH - VGL	-0.3 to + 46	V
Operating Temp. Range	TOTR	-30 to +85	°C
Storage Temperature	TSTG	-55 to +125	°C

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and affect its reliability.

6.2. Recommended Operating Range

Table 5. Recommended Operating Range (GND = 0V)

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (1)	-	VCC	1.7	3.0	3.6	V
Supply Voltage (2)	-	VPOS	10	-	15	V
Supply Voltage (3)	-	VNEG	-15	-	-10	V
Supply Voltage (4)	-	VGH	7.0	VGL + 42	VGL + 45	V
Supply Voltage (5)	-	VGL	-20	-	VNEG - 4	V
Clock Frequency (1)	-	fGCLK	-	-	200	KHz
Clock Frequency (2)	VCC = 2.5V ~ 3.6V	fCLK	-	-	60	MHz
	VCC = 1.7V ~ 2.5V				45	
Operating temperature	-	T _A	-20	-	75	°C

6.3. Supply Capacitor Selection

We recommended it is necessary to connect 4.7µF ceramic capacitors from VCC, VGH, VGL, VPOS and VNEG to GND.

6.4. DC Characteristics

6.4.1. Source DC Characteristics (TA = 25°C, VCC=3.0V, GND = 0V, VPOS = 15V, VNEG = -15V, CLK=20MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V _{IH}	-	0.8 x VCC	-	VCC	V
Low level input voltage	V _{IL}	-	GND	-	0.2 x VCC	V
High level output voltage	V _{OH}	I _{OH} = 2mA	VCC-0.5V	-	VCC	V
Low level output voltage	V _{OL}	I _{OL} = 2mA	GND	-	GND+0.5V	V
Input leakage current	I _L	-	-1	-	+1	μA
Input pull high / low resistance	R _{PH} / R _{PL}	VCC = 1.8V	200	-	1000	KΩ
		VCC = 3.0V	100		450	
Logic static current, output inactive	I _{CCS}	When VPOS and VNEG = 0, V _{IN} = GND or VCC	-	-	30	μA
Logic current, output active	I _{CC1}	Per output that is switched to VNEG.	-	-	3	mA
VPOS DC current	I _{POS1}	Per output that is switched to VPOS.	-	-	30	μA
VNEG DC current	I _{NEG1}	Per output that is switched to VNEG.	-	-	30	μA
VPOS Switching current	I _{POS2}	VPOS = 15V, VNEG = -15V, Cload = 100pf, f _{LINE} = 57KHz	-	-	90	mA
VNEG Switching current	I _{NEG2}	VPOS = 15V, VNEG = -15V, Cload = 100pf, f _{LINE} = 57KHz	-	-	90	mA

6.4.2. Gate DC Characteristics (TA = 25°C, VCC=3.0V, GND = 0V, VGH = 22V, VGL = -20V, GCLK=200KHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V _{IH}	-	0.8 x VCC	-	VCC	V
Low level input voltage	V _{IL}	-	0	-	0.2 x VCC	V
High level output current	I _{XOH}	Driving current, V _O = VGH - 0.5V	0.5	-	-	mA
Low level output current	I _{XOL}	Sink current, V _O = VGL + 0.5V	-0.5	-	-	mA
Input Leakage current	I _{IL}	-	-1	-	1	μA
Input pull high / low resistance	R _{PH} / R _{PL}	VCC = 1.8V	200	-	1000	KΩ
		VCC = 3.0V	100		450	
Operating current consumption (Note 1)	I _{CC}	VCC = 3.0V Fclk = 20KHz, No load	-	-	120	μA
Operating current consumption (Note 1)	I _{GH}	VGH = 22V, Fclk = 20KHz, No load	-	-	300	μA
Operating current consumption (Note 1)	I _{GL}	VGL = -20V Fclk = 20KHz, No load	-	-	300	μA

Note 1: For STV frequency = 60 Hz and two pulse mode

6.5. AC Characteristics

6.5.1. Source AC Characteristic (TA = 25°C, VCC=3.0V, GND = 0V, VPOS = 15V, VNEG = -15V,VGL= -20V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock CLK cycle time	t_{cy}	-	16.67	50	-	nS
D7...D0 setup time	t_{su}	-	8	-	-	nS
D7...D0 hold time	t_h	-	8	-	-	nS
STL1/STL2 setup time	t_{stls}	-	$0.5 \times t_{cy}$	-	$0.8 \times t_{cy}$	nS
STL1/STL2 hold time	t_{stlh}	960 outputs	$0.5 \times t_{cy}$	-	$240 \times t_{cy} - t_{stls}$	nS
		800 outputs			$200 \times t_{cy} - t_{stls}$	
		720 outputs			$180 \times t_{cy} - t_{stls}$	
		640 outputs			$160 \times t_{cy} - t_{stls}$	
GLOSTL setup time	$t_{glostls}$	-	$0.5 \times t_{cy}$	-	$0.8 \times t_{cy}$	nS
GLOSTL hold time	$t_{glostlh}$	960 outputs	$0.5 \times t_{cy}$	-	$240 \times t_{cy} - t_{stls}$	nS
		800 outputs			$200 \times t_{cy} - t_{stls}$	
		720 outputs			$180 \times t_{cy} - t_{stls}$	
		640 outputs			$160 \times t_{cy} - t_{stls}$	
LE on delay time	t_{LEdy}	-	$3.5 \times t_{cy}$	-	-	nS
LE high-level pulse width	t_{LE}	VCC=2.5V to 3.6V	300	-	-	nS
LE off delay time	t_{LEoff}	-	200	-	-	nS
Output settling time to +/- 30mV	t_{OUT}	Clload = 200pF	-	-	20	μ S

(TA = 25°C, VCC=1.8V, GND = 0V, VPOS = 15V, VNEG = -15V, VGL= -20V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock CLK cycle time	t_{cy}	-	22.22	-	-	nS
D7...D0 setup time	t_{su}	-	11	-	-	nS
D7...D0 hold time	t_h	-	11	-	-	nS
STL1/STL2 setup time	t_{stls}	-	$0.5 \times t_{cy}$	-	$0.8 \times t_{cy}$	nS
STL1/STL2 hold time	t_{stlh}	960 outputs	$0.5 \times t_{cy}$	-	$240 \times t_{cy} - t_{stls}$	nS
		800 outputs			$200 \times t_{cy} - t_{stls}$	
		720 outputs			$180 \times t_{cy} - t_{stls}$	
		640 outputs			$160 \times t_{cy} - t_{stls}$	
GLOSTL setup time	$t_{glostls}$	-	$0.5 \times t_{cy}$	-	$0.8 \times t_{cy}$	nS
GLOSTL hold time	$t_{glostlh}$	960 outputs	$0.5 \times t_{cy}$	-	$240 \times t_{cy} - t_{stls}$	nS
		800 outputs			$200 \times t_{cy} - t_{stls}$	
		720 outputs			$180 \times t_{cy} - t_{stls}$	
		640 outputs			$160 \times t_{cy} - t_{stls}$	
LE on delay time	t_{LEdy}	-	$4.5 \times t_{cy}$	-	-	nS
LE high-level pulse width	t_{LE}	VCC=1.7V to 2.5V	400	-	-	nS
LE off delay time	t_{LEoff}	-	250	-	-	nS
Output settling time to +/- 30mV	t_{OUT}	Clload = 200pF	-	-	20	μ S

6.5.2. Gate AC Characteristic (TA = 25°C, VCC = 3.0V, GND = 0V, VGH = 22V, VGL = -20V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock rise time	Trck	10% to 90%	-	-	100	nS
Clock fall time	Tfck	90% to 10%	-	-	100	nS
Clock pulse width (low)	Tckl	-	500	-	-	nS
Clock pulse width (high)	Tckh	-	500	-	-	nS
Clock frequency	Fclk	-	-	-	200	KHz
XON pulse width	t _{WXON}	-	10	-	-	µs
XON to output delay time	t _{PD}	CL=300pF	-	-	20	µs
STV rise time	Trstv	10% to 90%	-	-	100	nS
STV fall time	Tfstv	90% to 10%	-	-	100	nS
STV setup to Clock	Tsu	-	100	-	Tckh-100	nS
STV hold from Clock	Th	-	100	-	Tckh-100	nS
Output transfer delay time	Td	CL = 300pf,	-	3	-	uS
Output rise time	Tr	CL = 300pf, 10% to 90%	-	-	1	uS
Output fall time	Tf	CL = 300pf, 90% to 10%	-	-	1	uS
VCC rise time	Ton	-	-	-	20	ms
VCC fall time	Toff	-	-	-	20	ms
VCC waiting time	Toff-on	-	700	-	-	ms

(TA = 25°C, VCC = 1.8V, GND = 0V, VGH = 22V, VGL = -20V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock rise time	Trck	10% to 90%	-	-	100	nS
Clock fall time	Tfck	90% to 10%	-	-	100	nS
Clock pulse width (low)	Tckl	-	1000	-	-	nS
Clock pulse width (high)	Tckh	-	1000	-	-	nS
Clock frequency	Fclk	-	-	-	200	KHz
XON pulse width	t _{WXON}	-	10	-	-	µs
XON to output delay time	t _{PD}	CL=300pF	-	-	20	µs
STV rise time	Trstv	10% to 90%	-	-	100	nS
STV fall time	Tfstv	90% to 10%	-	-	100	nS
STV setup to Clock	Tsu	-	100	-	Tckh-100	nS
STV hold from Clock	Th	-	100	-	Tckh-100	nS
Output transfer delay time	Td	CL = 300pf,	-	3	-	uS
Output rise time	Tr	CL = 300pf, 10% to 90%	-	-	1	uS
Output fall time	Tf	CL = 300pf, 90% to 10%	-	-	1	uS
VCC rise time	Ton	-	-	-	20	ms
VCC fall time	Toff	-	-	-	20	ms
VCC waiting time	Toff-on	-	700	-	-	ms

6.6. Operating Timing

6.6.1. Source

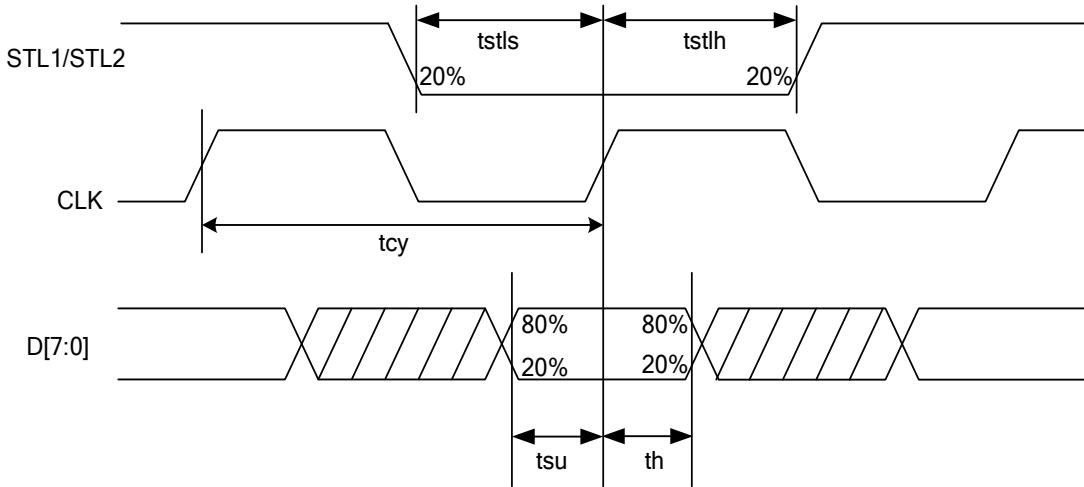


Figure 4. Clock and Data Timing

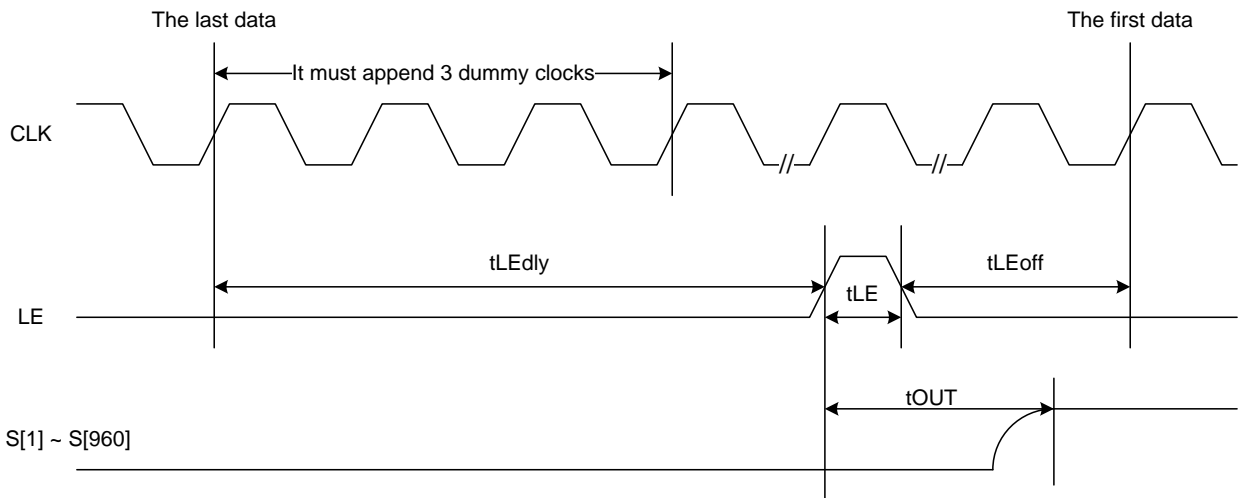


Figure 5. Output Latch / Control Signals

Note: After the last data, CLK must append 3 dummy clocks at least.

6.6.2. Gate

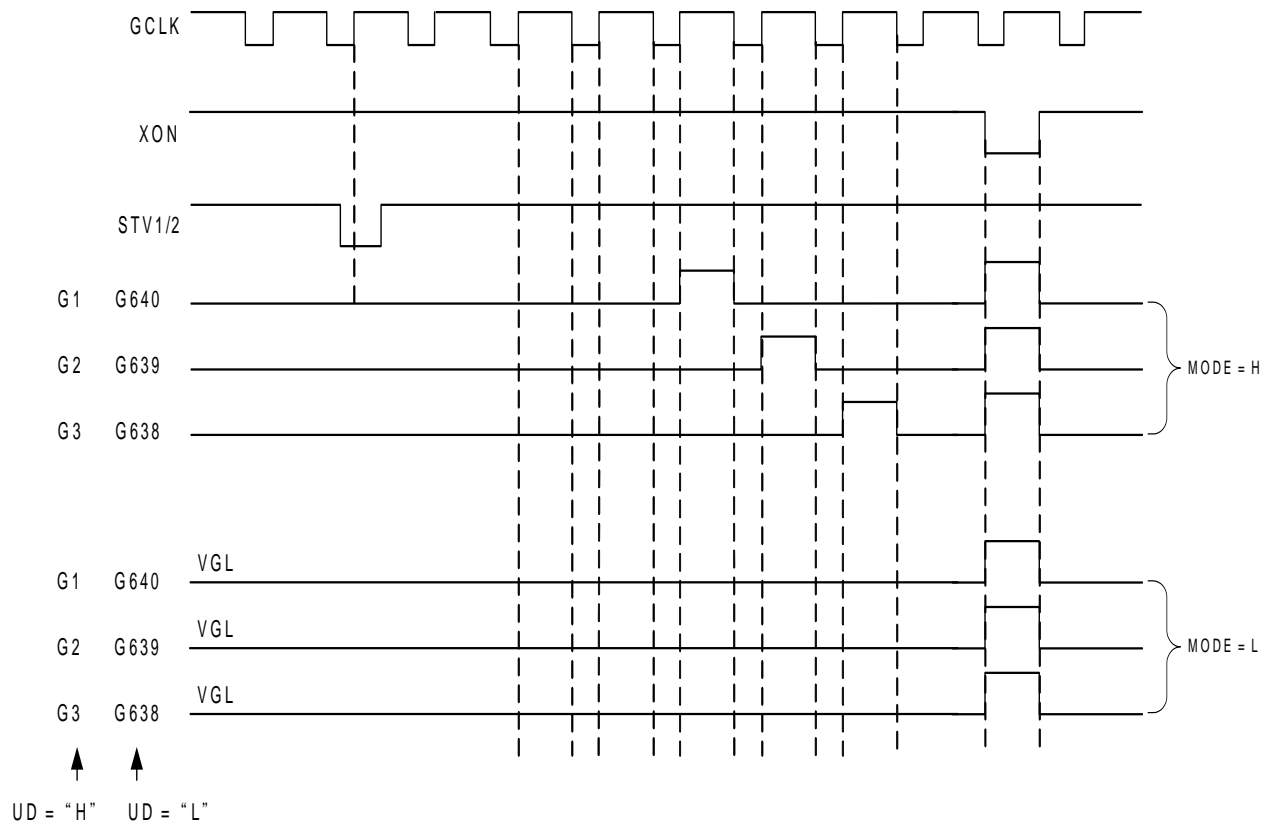


Figure 6. Example of input/output timing

6.7. Timing Waveform

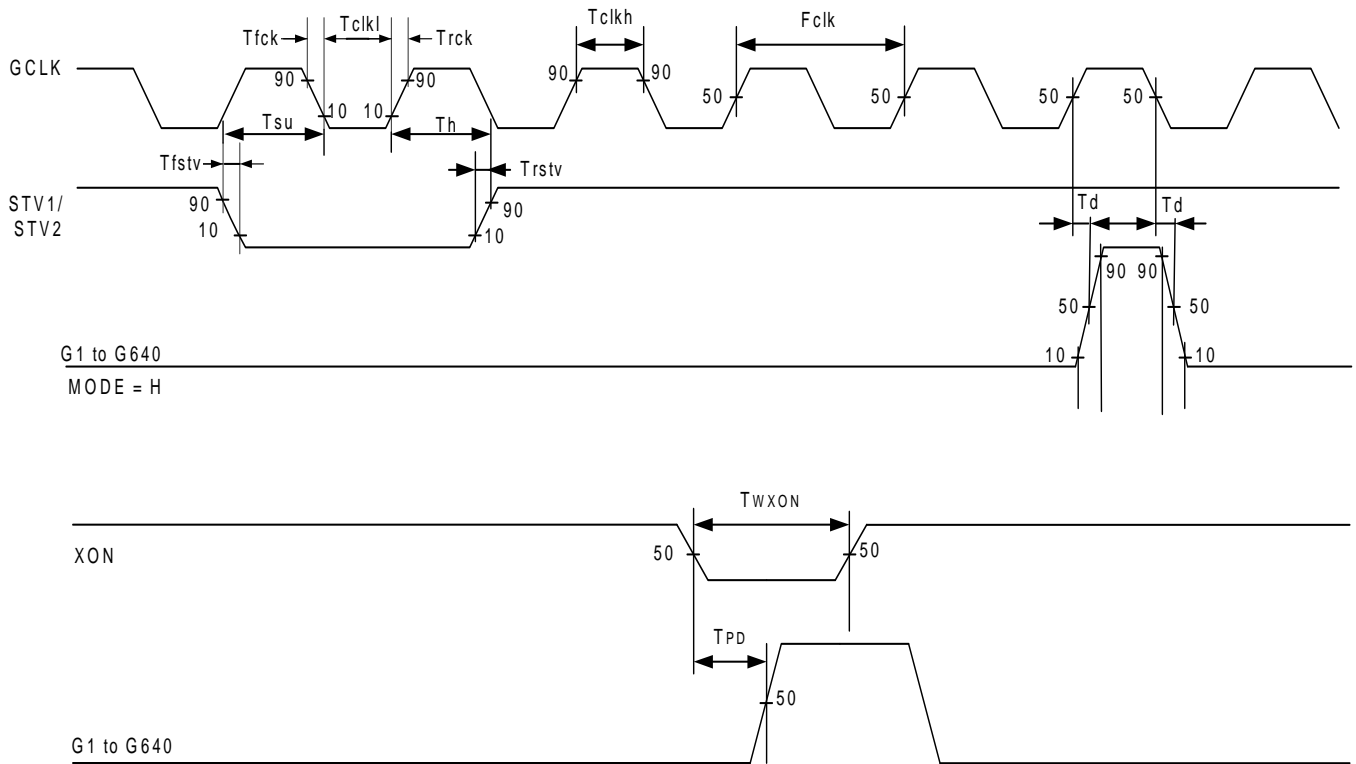


Figure 7. Timing Waveform

6.8. VCC on/off time

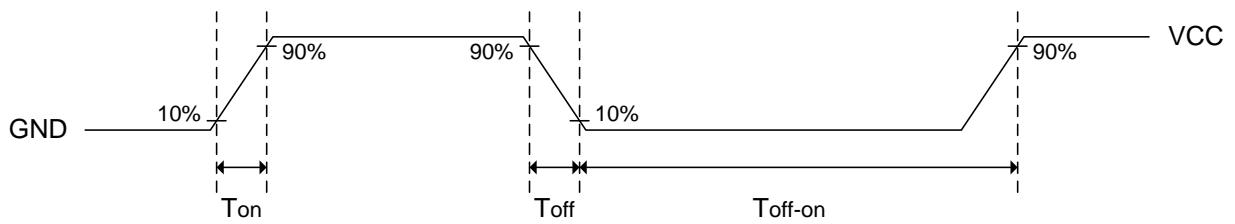


Figure 8. VCC on/off time

7. DEFINITIONS

7.1. Data Sheet Status

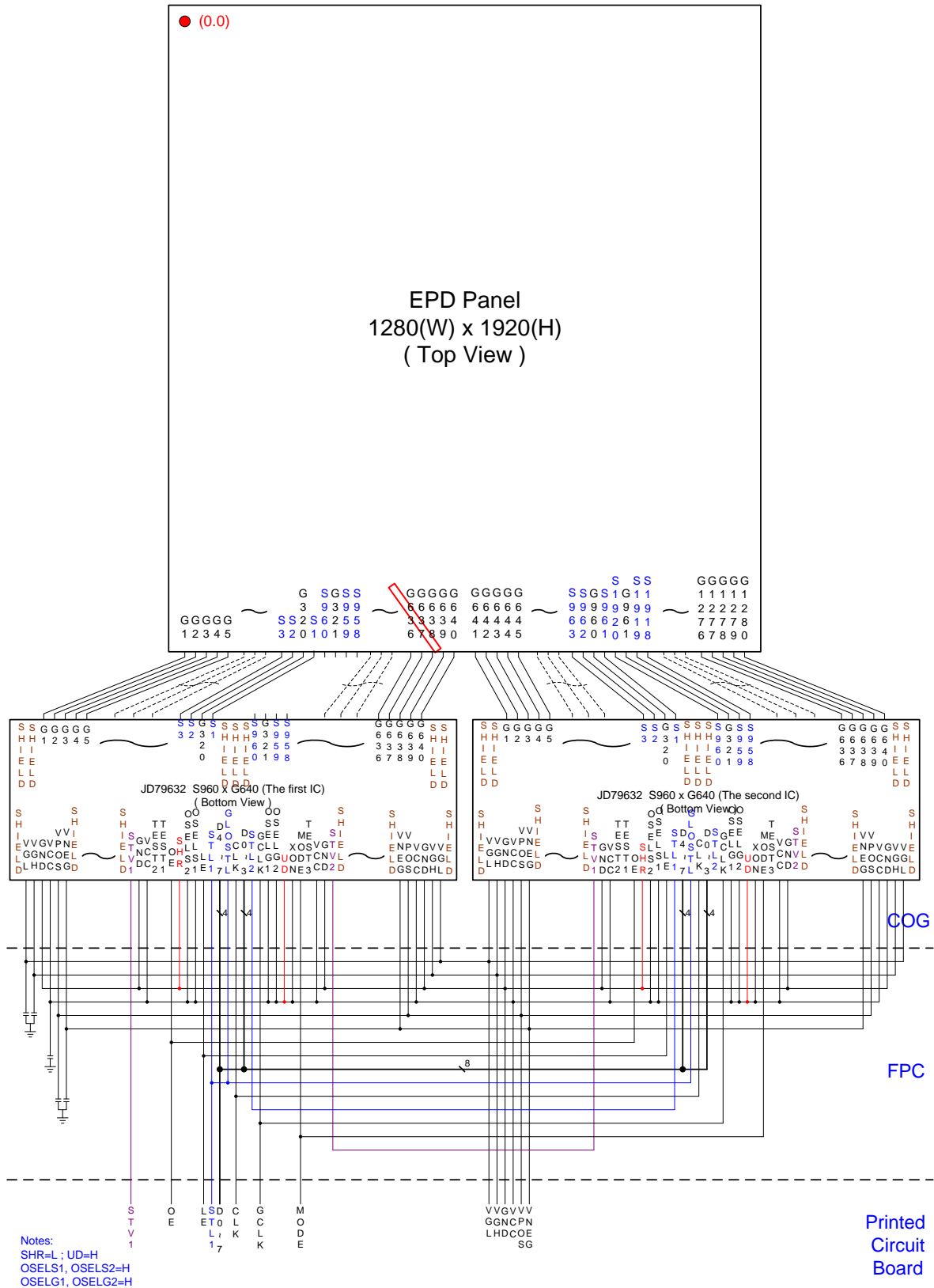
Tentative Data Sheet	This data sheet contains Tentative data; supplementary data may be published later.
Data Sheet	This data sheet contains final product specifications.

Contents in the document are subject to change without notice.

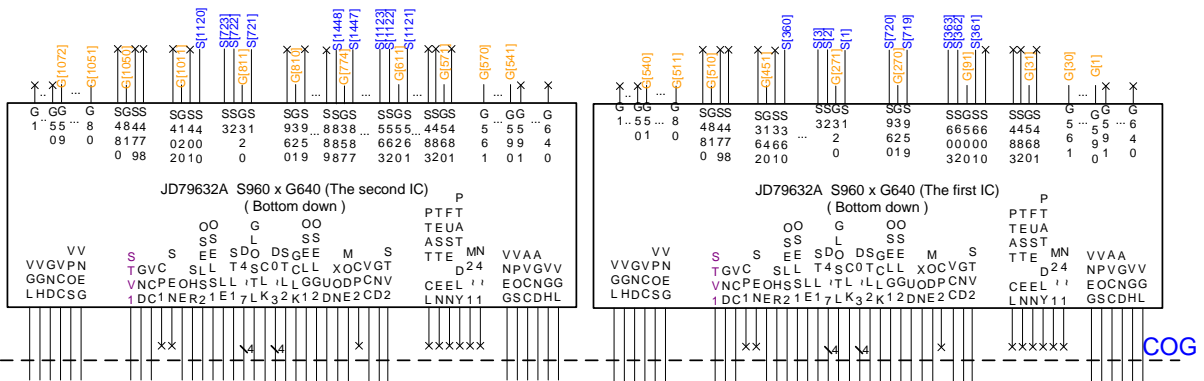
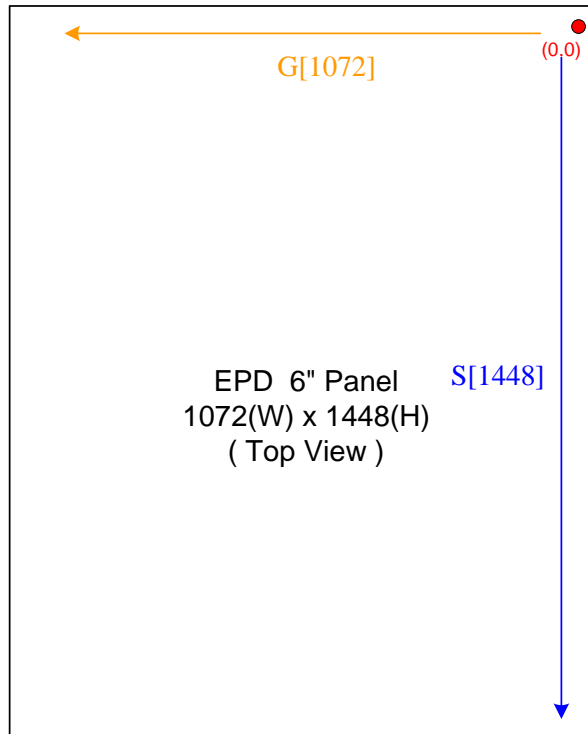
7.2. Life Support Application

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Fitipower customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify fitipower for any damages resulting from such improper use or sale.

The connection example when the EPD panel of 1280(W) x 1920(H) is composed by cascade using the EPD driver (EK79632A) as shown.



The connection example when the EPD panel of 1072(W) x 1448(H) is composed by cascade using the EPD driver (EK79632A) as shown.



Notes:
 SHR=L ; UD=L
 1st IC OSELS1=L, OSELS2=H
 2nd IC OSELS1=H, OSELS2=L
 OSELG1=L, OSELG2=H